

**REMARKS**

Claims 1-6 were examined on their merits. Claims 7-8 have been restricted out of the present application in favor of a later-filed divisional application.

*Formal Matters*

1. The Examiner indicates that claims 3-4 and 6 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicant respectfully holds the rewriting in abeyance until the arguments with respect to independent claim 1 have been considered.

*Art Rejections*

1. Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mochizuki et al., U.S. Patent No. 4,313,180 ("Mochizuki") in view of Abe et al., U.S. Patent No. 6,018,802 ("Abe `802"). Claim 1 is an independent claim. Applicant respectfully traverses this rejection for at least the reasons stated below.

In a non-limiting embodiment of the present invention, a data backup apparatus for use with on-vehicle equipment such as a car navigation system is provided. Specifically, a dynamic RAM (DRAM) having a plurality of memory areas is provided. A detection unit detects the state of the power supply such that when the switch of a vehicle key is in the ON position, the power is fed from the step-up/down power supply to the CPU and DRAM. When the switch is changed to the OFF position, the power supply detection unit detects a power OFF command. The CPU

then sets the DRAM into a self-refresh mode to prevent the loss of data stored in DRAM. After switching the DRAM to self-refresh mode, the control unit switches the power supply source from the step-up/down power supply to the backup power supply. In short, the refreshing mode is not dependent on the operative state of the CPU.

Mochizuki, on the other hand, is drawn to a refresh system for a dynamic memory wherein a refresh control circuit is connected to receive power from the backup battery included in an electronics apparatus (See Abstract). Specifically, when the main power is applied to the electronics apparatus, the DRAM receives a first refresh control signal derived from the CPU. However, when the main power supply is interrupted, the DRAM receives a second refresh control signal derived from the refresh control circuit which is operated by a small battery.

The Examiner acknowledges that Mochizuki fails to disclose at least the following recitations of independent claim 1:

control means for arbitrarily changing, regardless of the operative state of a CPU, said dynamic RAM to a self refresh mode when said detection means detects the OFF command of the main power supply, and feeding power from a backup power supply to said dynamic RAM.

Therefore, the Examiner relies on Abe to fulfill at least the above deficiencies of Mochizuki.

Abe is drawn to a communication apparatus having power backup functions for image memory (See e.g., Title). Specifically, a facsimile apparatus comprises a main power supply unit 15 for controlling the energization to respective units of the facsimile apparatus I (See Col. 8, lines 37-44). While the main power supply 16 rises, the secondary battery 19 is continuously

charged (See Col. 8, lines 25-26). The main power supply 16 is activated by a call signal from a telephone so that the power consumption in stand-by mode is made substantially zero (See Col. 2, lines 2-5).

The Examiner appears to assert that the main power supply control unit is equivalent to the claimed control means for arbitrarily changing the dynamic RAM to a self-refresh mode regardless of the operative state of the CPU. The Examiner relies on Col. 2, lines 47-51 to support his assertion. This passage in Abe, however, simply gives a generic definition for the self-refreshing mode of a DRAM and its basic use. The passage does not described a control means for arbitrarily changing, regardless of the operative state of the CPU, a dynamic RAM to a self refresh mode.

Furthermore, Applicant submits that Figure 8 of Abe clearly depicts and respectively describes the DRAM 4 being dependent on the state of the CPU. Specifically, as illustrated in Figure 8 and described in Col. 7, lines 61-67 and Col. 8, lines 1-35, when AC input ceases, the CPU is reset (step 401), the control of the DRAM is switched from the CPU to the microcomputer and set to self fresh mode (step 403). When the CPU is initialized (step 409), the control of the DRAM is switched from the microcomputer to the CPU and refreshment of the DRAM is normalized. (See Col 7, lines 62-67 and Col. 8, lines 1-23). Clearly, the refreshment mode of the DRAM is dependent upon the operative state of the CPU (either being initialized or reset). Thus, absent from Abe is any description or suggestion of a control means for arbitrarily changing, regardless of the operative state of a CPU, said dynamic RAM to a self-refresh mode.

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Without at least such a suggestion, one would not have been (and could not have been) motivated to combine the refresh system for a dynamic memory, as disclosed in Mochizuki, with the communication apparatus having a power backup function for image memory, as taught in Abe, to produce the claimed subject matter. Because there can be found in Abe no teaching or suggestion that meets the above-identified limitations, the combination of Mochizuki and Abe cannot reasonably be said to render obvious the claimed subject matter. The Examiner is therefore respectfully requested to withdraw the § 103(a) rejection from independent claim 1.

2. Claims 2 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mochizuki and Abe, and further in view of Abe, U.S. Patent No. 5,590,082 ("Abe `082").

Claims 2 and 5 depend from independent claim 1. Mochizuki is deficient with respect to claim 1 for at least the reasons stated above. Therefore, the Examiner must rely on Abe `082 to compensate for the foregoing deficiencies.

Abe `082 is directed to a memory control circuit capable of reliably carrying out self-refresh starting operations to establish a self-refresh mode for a DRAM when the power supply is lowered. Abe `082, however, fails to disclose the above-identified recitations with respect to independent claim 1. Therefore, Applicant submits that claims 2 and 5 are patentable at least by virtue of their dependency. The Examiner is therefore respectfully requested to withdraw the § 103(a) rejection.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

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Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

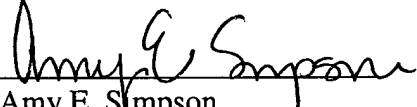
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